Claim Amendments

Please amend claims 1, 10, 14, and 18 as follows:

Please cancel claim 3 as follows:

Please add new claim 24 as follows:

1. (currently amended) A method for forming a dual damascene opening to protect a low-K dielectric insulating layer from an ashing process comprising the steps of:

providing a semiconductor process wafer comprising a via opening extending though a thickness portion of at least one dielectric insulating layer;

depositing a first dielectric layer stack ~~layer~~ comprising at least one dielectric layer over the at least one dielectric insulating layer to seal the upper portion of the via opening;

blanket depositing a second dielectric layer stack comprising at least one dielectric layer to form a hardmask over and contacting the first dielectric layer stack;

photolithographically patterning an overlying photoresist layer and reactive ion etching through a thickness of the hardmask and the first dielectric layer stack to form a trench opening etching pattern overlying and encompassing the via opening while leaving the via opening sealed; ~~and,~~

removing the photoresist layer according to an ashing process with the via opening sealed; and,

reactive ion etching through a thickness portion of the at least one dielectric insulating layer to form a dual damascene opening.

2. (original) The method of claim 1, wherein the step of depositing the first dielectric layer stack forms a substantially planar upper surface.

3. cancelled

4. (original) The method of claim 1, wherein the at least one dielectric insulating layer comprises a low-K inter-metal dielectric (IMD) layer having a dielectric constant of less than about 2.5.

5. (original) The method of claim 4, wherein the low-K IMD layer is selected from the group consisting of carbon doped silicon oxide, organo-silicate glass, spin-on carbon doped glass, and silsesquioxanes.

6. (original) The method of claim 4, wherein the at least one dielectric insulating layer consists essentially of the low-K IMD layer and an overlying dielectric anti-reflective coating (DARC) layer selected from the group consisting of silicon oxynitride, and silicon oxycarbide.

7. (original) The method of claim 1, wherein the first and second dielectric layer stacks are formed according to a first and second CVD process respectively.

8. (original) The method of claim 7, wherein the first CVD process comprises a CVD deposition process comprising at least one of a lower temperature and a higher pressure compared to the second CVD process.

9. (original) The method of claim 8, wherein the first CVD process is selected form the group consisting of atmospheric CVD and plasma enhanced CVD.

10. (currently amended) The method of claim 7, wherein the first CVD process comprises a non-conformal deposition process ~~to carry out deposition of at least a lower portion of the first~~

~~dielectric layer stack~~ to selectively seal an upper portion of the via opening while forming a keyhole in a lower portion of the via opening.

11. (original) The method of claim 1, wherein the first dielectric layer stack comprises the at least one dielectric layer selected from the group consisting of silicon dioxide, silicon nitride, silicon oxynitride, silicon oxycarbide, and hydrogenated silicon oxycarbide.

12. (original) The method of claim 1, wherein the second dielectric stack comprises the at least one dielectric layer selected from the group consisting of silicon nitride, silicon oxynitride, and silicon oxycarbide.

13. (original) The method of claim 1, further comprising carryout a subsequent reactive ion etching process to remove a remaining portion of the first and second dielectric layer stacks while removing a barrier layer disposed at the via opening bottom portion to form closed communication with an underlying conductive area.

14. (currently amended) A method for forming a copper filled dual damascene formed in a low-K dielectric insulating layer to prevent ~~carbon depletion~~ damage during an ashing process comprising the steps of:

providing a semiconductor process wafer comprising a via opening extending though a thickness portion of at least one dielectric insulating layer;

depositing a first dielectric layer stack ~~layer~~ comprising at least one dielectric layer according to a first CVD process ~~comprising at least one dielectric layer~~ over the ~~at least one dielectric insulating~~ via opening to close off and selectively seal an upper portion of the via opening ~~and form a substantially planar upper first dielectric layer stack surface~~;

depositing a second dielectric layer stack according to a second CVD process comprising at least one dielectric layer to form a hardmask over and contacting the first dielectric layer stack;

~~depositing a photoresist layer and~~ photolithographically patterning an overlying photoresist layer and reactive ion etching through a thickness of the hardmask and the first dielectric layer stack to form a trench opening etching pattern overlying and encompassing the via opening while leaving the via opening sealed;

carrying out a plasma ashing process to remove the photoresist layer without exposing an interior portion of the via opening; and,

etching according to a second reactive ion etching process through a thickness portion of the at least one dielectric insulating layer to form a dual damascene opening.

15. (original) The method of claim 14, wherein the at least one dielectric insulating layer comprises a low-K IMD layer having a dielectric constant of less than about 2.5.

16. (original) The method of claim 15, wherein the low-K IMD layer is selected from the group consisting of carbon doped silicon oxide, organo-silicate glass, spin-on carbon doped glass, and alkyl substituted silsesquioxanes.

17. (original) The method of claim 14, wherein the at least one dielectric insulating layer consists essentially of the low-K IMD layer and an overlying dielectric anti-reflective coating (DARC) layer selected from the group consisting of silicon oxynitride and silicon oxycarbide.

18. (currently amended) The method of claim 14, wherein the first CVD process comprises non-conformal deposition of at least a

portion of a lowermost dielectric layer of the first dielectric layer stack ~~to close off the upper portion of the via opening~~ to selectively seal an upper portion of the via opening while forming a keyhole in a lower portion of the via opening.

19. (original) The method of claim 14, wherein the first CVD process comprises at least one of a lower deposition temperature and a higher pressure compared to the second CVD process to produce a lower etching resistance in a reactive ion etching process.

20. (original) The method of claim 14, wherein the first dielectric stack comprises at least one dielectric layer selected from the group consisting of silicon dioxide, silicon nitride, silicon oxynitride, silicon oxycarbide, and hydrogenated silicon oxycarbide.

21. (original) The method of claim 14, wherein the second dielectric stack comprises at least one dielectric layer selected from the group consisting of silicon nitride, silicon oxynitride, and silicon oxycarbide.

22. (original) The method of claim 14, further comprising a subsequent reactive ion etching process to remove a remaining

portion of the first and second dielectric layer stacks while etching through a barrier layer disposed at the via opening bottom portion to form closed communication with and underlying copper conductive area.

23. (original) The method of claim 22, further comprising depositing and planarizing a copper layer to fill the dual damascene opening.

24. (new) The method of claim 1, wherein the step of depositing a first dielectric layer stack to seal the upper portion of the via opening forms a keyhole within a lower portion of the via opening.